REMARKS

The Examiner's Final Office Action mailed on December 14, 2004 has been received and its contents carefully considered.

Claims 1, 2, 4-7 and 10-18 are currently pending in this application. Claims 1, 6 and 7 are independent claims.

The applicant acknowledges with appreciation the Examiner's indication that claims 6, 7, 10-15, 17 and 18 are allowed, and that claim 5 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

In the Final Action, claims 1, 4 and 16 are rejected under 35 U.S.C. §102(b) as being anticipated by Watson (U.S. Patent No. 5,034,814). Claim 2 is rejected under 35 U.S.C. §103(a) as being obvious over Watson. The rejections are respectfully traversed.

The Watson reference cited by the Examiner is directed to a system for converting a high definition video signal corresponding to a high-definition picture, into a sub-sampled video signal compatible with NTSC transmission by outputting the NTSC samples in a manner which preserves in the NTSC signal the relative frame-to-frame geometric offsets used in the sampling process, thereby minimizing NTSC flicker on conventional NTSC receivers (see Abstract). In the Final Action, the examiner asserts Watson discloses all of the claimed subject matter. The applicant respectfully disagrees.

For example, the Examiner points to the counter 132 in Figure 21 of Watson as corresponding to the counter circuit recited in claim 1. In Watson, the counter 132 receives an output of a pixel rate clock 130 that is provided with an HD sync signal (see column 15, lines 10-11). The HD sync signal is separated from a composite HD video signal and is used for locking the pixel rate clock to the HD signal frame rate (see column 15, lines 11-13). Therefore, the counter 132 cannot count a pixel number of each line in the input data, as claim 1 requires, because the HD video signal itself is not applied to the counter 132. The counter 132 in Watson is shown in Figure 21 as a simple divide-by-two counter and clearly has a very different function from that of the counter circuit of claim 1.

In addition, the Examiner points to the switch control circuit 49 in Figure 21 of

Watson as corresponding to the judgment circuit recited in claim 1. Since the switch control circuit 49 is connected to the pixel rate clock 130, the switch control circuit may respond to a pixel number generated by the pixel rate clock 130. However, as discussed above, the pixel rate clock 130 does not receive the input data, but receives only the HD sync signal. Therefore, the switch control circuit 49 cannot calculate the difference between a standard number of pixels in a line and the pixel number counted by the counter circuit, as claim 1 requires. That is, the switch control circuit 49 is clearly different from the judgment circuit of claim 1.

Further, the Examiner points to the switch 51 in Figure 21 of Watson as corresponding to the selector recited in claim 1. But, the switch 51 simply switches between first and second positions so as to select different delays and attenuations to apply to the inputted HD signal data (see, for example, column 12, a line 63-67). The switch 51 cannot combine the delayed input data to generate as an output data, combined input data having the standard number of pixels, as claim 1 requires. Therefore, the switch 51 is clearly different from the selector of claim 1.

To summarize, Watson discloses that the counter 132 receives the output of the pixel rate clock 130 and the reset signal from the HD sync separator 47′ and controls the output switch 51 via the switch control circuit 49′ so that processing is applied to those pixels with vertical offset but is not applied to those with no vertical offset (see column 15, lines 11-17). The purpose of the circuit shown in Figure 21 of Watson is to carry out a vertical sub-sampling method on the pixels in different scan lines of an HD video signal so as to generate an NTSC signal (see column 15, lines 3-5). On the other hand, the claimed invention has a very different function and purpose, namely, to generate an output video data that has a standard number of pixels in each scan line by selectively combining delayed versions of the same input scan line data. As discussed above, the elements of the claimed invention are correspondingly different from those of the prior art reference. Thus, is respectfully submitted that claim 1, as well as claims 4 and 16, patentably distinguish over the applied prior art.

With regard to claim 2, the Examiner takes official notice that it is notoriously well known in the art to construct a delay circuit from a plurality of flip-flops, and therefore it would have been obvious to one skilled in the art at the time the invention

was made to modify the system of Watson by providing a plurality of flip-flop circuits in order to utilize a reliable circuit and cut the cost of the overall system as well. The Applicant respectfully submits that the modification suggested by the Examiner does not overcome the deficiencies in the base reference discussed above. Thus, even if the modification proposed by the Examiner were suggested by the prior art (which the Applicant does not admit), the application of the modification to Watson would not yield the claimed invention.

For at least the foregoing reasons, it is respectfully requested that the application be reconsidered and that the final rejections of pending claims 1, 2, 4 and 16 be withdrawn. Notice of allowance and passing of this application to issue with pending claims 1, 2, 4-7 and 10-18, is earnestly solicited.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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